REMARKS

Claims 1-14 and 27-38 are pending in this application. Claims 15-26 are canceled. Claims 27-38 are new. Claims 1, 2, 5, 6, 10 and 11 are currently amended. The specification and the drawings are also currently amended.

The amendments to the specification, drawings, and claims do not introduce new matter, and their entry is respectfully requested. The amended and new claims are supported in the specification and figures as follows. The amendment to claim 1 is supported in the specification at, e.g., page 5, lines 7-10. Claims 6 and 10 have been rewritten in independent form by incorporating all the limitations of their parent claim 1. Claims 2, 5, 6, and 11 have been amended to correct minor informalities.

New claims 31 and 32 are copies of claim 14 but are dependent on claims 1 and 6, respectively. New claim 27 is supported in the specification at, e.g., page 4, lines 30-34. Claims 33 and 38 are copies of claim 27 but are dependent on claims 6 and 10, respectively. New claims 28 and 29 are supported in the specification at, e.g., page 4, lines 17-24; and at, e.g., page 7, lines 22-28. New claims 34 and 35 are copies of claims 28 and 29, respectively, but are dependent on claims 33 and 34, respectively. New claim 30 is supported in the specification at, e.g., page 4, lines 17-24. New claim 37 is a copy of claim 30 but is dependent on claim10. New claim 36 combines the elements of claims 3 and 5 and is dependent on claim 6.

Amendments to the specification are supported as follows. The amendments to the paragraphs beginning on page 6, line 36 and on page 9, line 14 are supported at, e.g., page 1, lines 34-37; page 6, lines 2-3; and reference 6 in Fig. 1. The amendments to the paragraphs beginning on page 8, lines 18 and 31 are supported at, e.g., page 2, lines 24-26; page 4, lines 17-24; page 6, lines 29-33; 34-37; page 6, lines 2-3; reference 6 in Fig. 1; and Figs. 4 and 6 especially at reference number 40. These amendments change the specification to make reference to Figs. 2A, 2B, 2C, 3B, 3C and 5.

Amendments to the drawings are supported as follows. Amended reference numbers 41, 42, 51 and 52 are supported at, e.g., page 8, lines 1-4. Amended reference number 43 is supported at, e.g., page 8, lines 7-10. Amended reference numbers 53 is illustrated as hole 40 in Fig. 4 and described at page 9, lines 6-10.

ALLOWABLE SUBJECT MATTER

Claims 6-11, 14 and 32-38 are submitted to be allowable. The Examiner has found claims 6 and 10, both dependent from claim 1, to contain allowable subject matter. Accordingly, claims 6 and 10 have been amended to be in independent form by incorporating all limitations of their parent independent claim, claim 1, and are therefore submitted to be now allowable. Further, the claims depending from claim 6, namely claims 7-9 and 32-36, and the claims depending from claim 10, namely claims 11, 14, 37 and 38 are also allowable since they inherit all the patentable limitations of parent independent claims 6 and 10, respectively.

OBJECTIONS TO THE SPECIFICATION AND CLAIMS

The Examiner has objected to the specification contending that there is no description of layers 38, 82, 40, 50 and 62 that appear in Figs. 2A, 6, 3A, 3B and 3C, respectively. In response, it is submitted that the amendments to the specification and drawings obviate and overcome this objection, and its withdrawal is respectfully requested.

The Examiner has also objected to claims 2 and 11 contending that the use of "can" is an informality, and to claim 5 and 6 contending that there is a lack of clear antecedent basis. In response, it is submitted that the amendments to claims 2, 5, 6 and 11 obviate and overcome these objections, and their withdrawal is respectfully requested

REJECTIONS UNDER 35 U.S.C. § 102(B)

Claims 1-5 and 12-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sakaguchi et al. US patent 6,569,748 B1 ("Sakaguchi").[1]

In response, Applicants respectfully submit that Sakaguchi does not anticipate the claims because they recite, *inter alia*, producing semiconductor structures having pre-determined cavities in a sub-surface layer underneath a surface layer. On the other hand, Sakaguchi discloses only producing semiconductor structures with smooth surface layers and without any subsurface cavities. Further, Sakaguchi does not

[1] Applicants respectfully note that claim 14 should not have been rejected, since depends from claim 6 which has been found to contain allowable subject matter.

disclose or teach the etching of a subsurface layer which is necessary in order to produce pre-determined subsurface cavities.

The present invention discloses and claims methods that create cavities of limited and pre-determined extent in a subsurface layer within a semiconductor structure. The nature of the cavities produced can be readily appreciated by inspecting, e.g., cavity 40 in Fig. 2C, cavities 58 and 68 in Fig. 4, and cavities 88 and 98 in Fig. 5. They are seen to extend within pre-determined portions of a subsurface layer and are covered by a surface layer except for a hole for etchant access.

These cavities are produced by, first, implanting atoms within the subsurface layer in selected regions which are defined by masks. See, e.g., Fig. 2B. Since implanted regions are more easily etched than non-implanted regions, the recited cavities can be produced by selective etching of the implanted regions of the subsurface layer. The implanting and etching are selective at least in that only limited pre-determined regions of the subsurface layer are implanted and only the pre-determined implanted regions are etched to form subsurface cavities. See, e.g., page 8, lines 11-13.

In contrast, the methods disclosed and taught in Sakaguchi do not produce determined cavities in a subsurface layer of a finished semi-conductor structure. The goal of Sakaguchi's methods is, instead, to produce a SOI semiconductor structure having a surface semiconductor layer that is uniform and of satisfactory quality throughout. See Sakaguchi at, e.g., col. 7, lines 28-35.

Figs. 1-6 in Sakaguchi illustrate the semiconductor structures and methods of this reference. No cavities at all are apparent in these figures. Also no cavities of determined and limited extent are disclosed or taught anywhere in Sakaguchi's specification. Sakaguchi simply does not disclose the pre-determined subsurface cavities recited in the claims. It is believed that the Examiner recognizes this as evidenced by the previously noted allowance of certain dependent claims.

Further, Sakaguchi's methods cannot produce the recited cavities at least because no etching a subsurface layer is disclosed or taught. In Sakaguchi, it is only the semiconductor surface layer that is etched in order to remove residual porous Si on the surface and to smooth irregularities in the surface. The limitations of

Sakaguchi's disclosure can be appreciated from the typical embodiment illustrated in Figs. 2A-F and described at col. 11, line 64 to col. 13, line 13.

The disclosed methods produce a first substrate having surface layer 13 of crystalline Si over subsurface layer 12 of porous Si, which is then bonded to second substrate 15 having surface oxide layer 14 (See, e.g., Fig. 2B). Upon separation of the bonded substrates in the plane of the porous layer, a SOI structure with crystalline surface layer 13 over subsurface oxide layer 14 results (See, e.g., Fig. 2D). Then and only is surface etching suggested to remove any retained porous Si (from layer 12) retained on the crystalline surface layer 13 and to smooth unacceptable surface irregularities (See, e.g., col. 13, lines 4-8; and col. 27, lines 51-56). Such finishing etching carried out across the entire surface layer.

Thus, Sakaguchi discloses etching carried out across the entire surface of a semiconductor structure, but does not disclose any of the subsurface etching necessary to produce cavities. Since Sakaguchi's goal is to produce an acceptable, uniform surface layer, subsurface etching and cavities are in fact to be avoided because they necessarily damage to some extent the surface layer.

In summary, the claims recite creating subsurface cavities by regionally selective implanting and etching of a subsurface layer. Sakaguchi discloses only producing a SOI structure with a smooth, uniform surface layer. This reference does not disclose, *inter alia*, these limitations, and thus cannot anticipate any of the claims. It is respectfully submitted that the rejections of independent claim 1, and of its dependent claims 2-5, 12, 13, 27-29 and 31, should be withdrawn.

CONCLUSION

In view of the above, the application is believed to be in condition for allowance, early notice of which would be appreciated. Should any issues remain, a personal or telephonic interview is respectfully requested to discuss the same in order to expedite the allowance of all the claims in this application.

Respectfully submitted,

(DWIGHT RENFREW, 38,594)

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